17.6 A 1V 18GHz Clock Generator in a 65nm PD-SOI Technology

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Advances in digital circuit design and the scaling of CMOS processes have ushered in the era of multi-gigahertz microprocessors. Recently, a double-precision floating-point unit running as high as 8GHz in a 90nm process was demonstrated [1]. Clocking such processors is challenging since this level of performance cannot be achieved using traditional circuit techniques. Moreover, each new technology node brings higher device variability and inferior analog performance, and these translate into increased jitter and smaller tuning ranges. The proposed PLL, based on a current-steering interpolating oscillator, achieves high-frequency operation and wide tuning range with minimal impact to circuit complexity.

The target floating-point unit, which is the next generation of [1], calls for an operating range of 8 to 12GHz at the nominal 1V supply across all process corners. These requirements place stringent specifications on the VCO design. A current-starved design [2,3] would typically be used in order to achieve a wide lock range. Unfortunately, current-starved techniques induce additional jitter, which is due to large VCO gains, and these designs have difficulty operating at high frequencies. An interpolating oscillator can significantly increase the maximum frequency of operation. The interpolating VCO PLL in [4] operated a maximum frequency of 9GHz and was fabricated in a 90nm SOI process. When simulated in a 65nm process, this design failed to meet the target tuning range across all process corners. The current-steering interpolating VCO shown in Fig. 17.6.1 is more robust. Each stage of the oscillator contains 4 inverting elements connected in parallel through control switches. When the control voltage (CT) is low, only the main inverter A drives the load of 4 inverters in the next stages. This effectively forms a 5-stage ring oscillator in a fanout-of-4 configuration. When CT is high, inverter B begins driving in parallel with inverter A, and the parallel combination of inverters AA and BB phase interpolate with inverters A and B. Simulations across process corners indicated that the combination of phase interpolation, as well as inverter drive strength, improves overall tuning range by 66% compared with the nominal design in [4].

The remaining components of the PLL are a phase frequency detector, charge pump, loop filter, and frequency divider. A high-speed phase frequency detector topology was used with circuit components tuned for speed. In particular, two high-speed dynamically pulsed D flip-flops were used for increased speed and robustness against process variation. Two precision delay lines were timed to minimize the dead zone. Two additional delay lines split the UP/DOWN signals into complements with minimal slew. The charge pump is a modified version of the circuit shown in [4]. The circuit comprises a current sink and source isolated from the loop filter via 2 switches. To ensure constant current throughout the operating region, the current source/sink transistors are bootstrapped to a fixed voltage. Dummy devices ensure equal loading on all signals seen at the output of the phase frequency detector. These devices also reduce the channel charge injected onto the loop filter by the switches. The charge-pump current is adjusted via a 3b code, which allows the selection of currents ranging from 8 to 64μA. A standard RC loop filter was implemented. Trimming bits were added to the resistor to allow for tuning after fabrication.

High V_t (HVT) and regular V_t (RVT) PLLs were designed and fabricated in a 65nm PD-SOI process [5]. Both PLLs used identical circuits with the exception of the transistor threshold voltages. The circuits were tested at the wafer level using a wedge probe with 3 RF pins and 5 power pins along with a 4-pin needle probe that provided the digital scan interface. A total of 120 HVT and RVT sites were tested across two 300mm wafers, with 3 HVT and 2 RVT sites excluded from the data set for failing to meet specifications, resulting in over 97% yield.

Figure 17.6.2 illustrates the lock ranges of the RVT PLLs as a function of supply voltage. The top family of curves is the composite of the maximum lock frequencies of the PLLs at each supply voltage. At the nominal supply voltage of 1V, the average maximum frequency was 18.1GHz with a standard deviation of 2.8GHz. The fastest part synthesized a maximum frequency of 24.6GHz at 1.0V and 36.0GHz at 1.6V. The bottom family of curves represents the minimum lock frequencies. The values in the center of the plot indicate the lock range (f_{max}/f_{min}) for the slowest maximum frequency and the fastest minimum frequency curves. At 1V, all 118 PLLs are able to lock target frequencies of 8 to 12GHz and a 2.0× or greater lock range is obtained at all supply voltages above 1.0V. The 117 HVT PLLs exhibited 6% lower average frequency, but a higher average lock range when compared with the RVT design. Figure 17.6.3 shows jitter across the lock range for both the RVT and HVT PLLs at 1V supply. The peaks in the 13 to 16GHz frequency band of these waveforms correspond to increased jitter exhibited by the test equipment feeding the external reference clock. The specified noise floor of the test equipment was 0.8ps. The minimum PLL jitter is $1.28ps_{rms}$ or $1.06ps_{rms}$, and occurs at 16.8GHz, or 11.5GHz, for the RVT and HVT PLLs, respectively. Figure 17.6.4 illustrates the PLL response to an instantaneous frequency step (16 to 8GHz) applied for various charge-pump currents and loop-filter resistances for the RVT PLL. The loop response is nearly critically damped about its nominal resistance value as shown in the inset. Figure 17.6.5 shows the static phase error of the HVT PLL at 1V supply as a function of the output frequency for full (64μA) and half (32μA) charge-pump currents. Over the 8 to 12GHz range, the static phase error is never worse than 2 degrees. Figure 17.6.6 summarizes the results for both PLLs.

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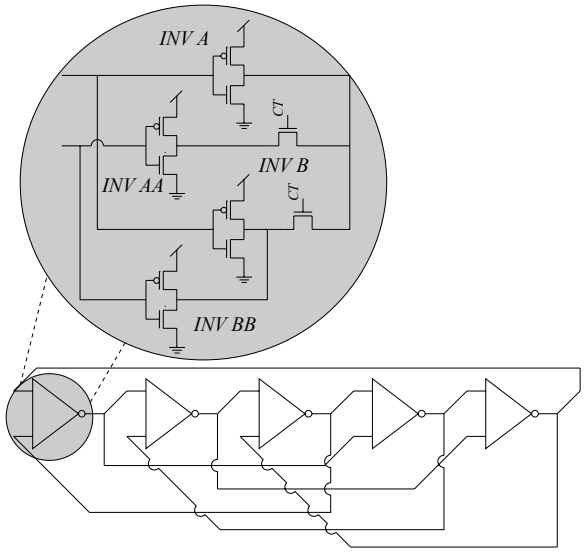

Figure 17.6.1: Current-steering interpolating ring oscillator.

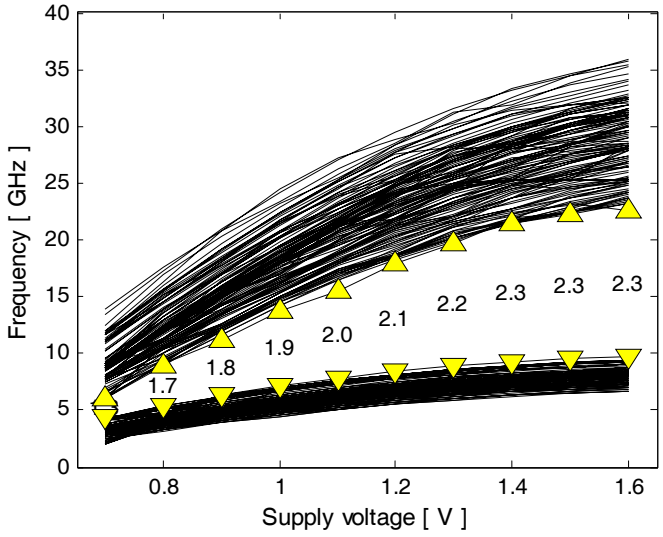

Figure 17.6.2: Lock ranges of all RVT PLLs versus supply voltage.

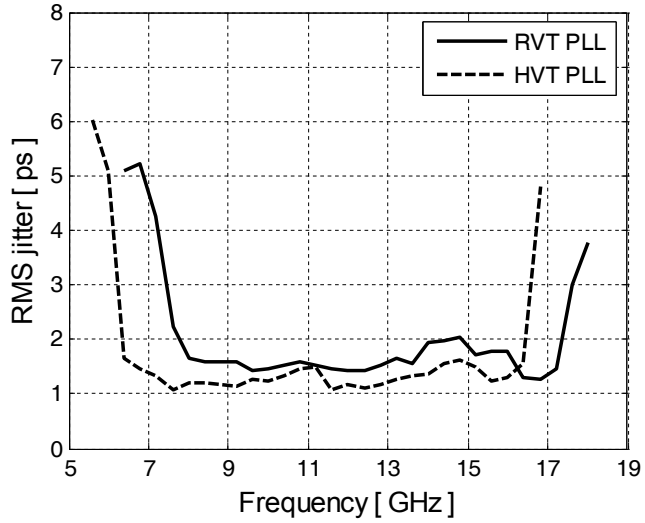

Figure 17.6.3: Measured RMS jitter at the output of the PLL across the lock range at 1.0V supply.

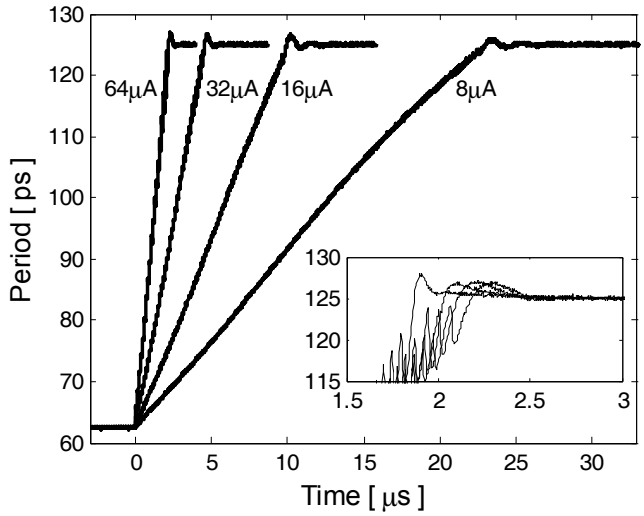

Figure 17.6.4: RVT PLL loop response to an instantaneous frequency step for various charge-pump currents. The inset illustrates loop dynamics at 64µA for 4 resistance settings, increasing left to right.

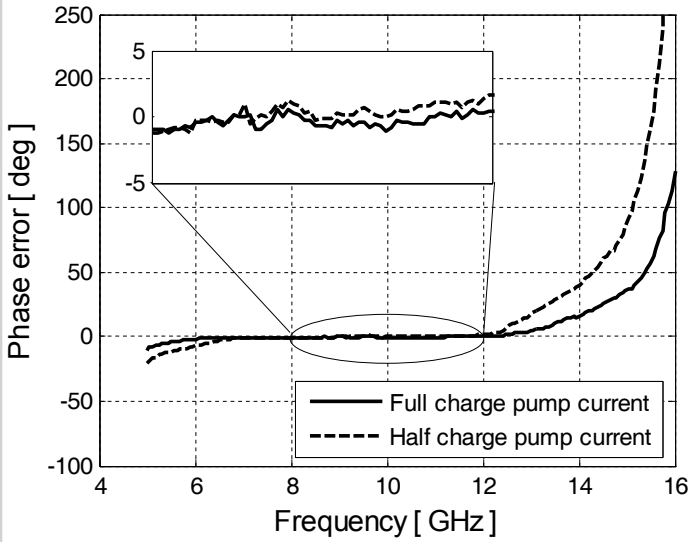

Figure 17.6.5: Measured static phase error of HVT PLL at 1.0V supply.

Parameter	HVT PLL	RVT PLL
Process Technology	PD-SOI 65nm: High V_t devices	PD-SOI 65nm: Regular V_t devices
Operating Supply Voltage Min/Max/Nominal (V)	0.7/1.6/1	0.7/1.6/1
PLL Area (mm^2)	0.18	0.18
Tuning Range Average of Yield @ 1.0V and 1.6V (GHz)	4.9-17.1 7.6-28.2	5.6-18.1 8.1-28.6
Minimum Jitter @ 1.0V (ps_{rms})	1.06	1.28
Multiplication Factor Range	8-64	8-64
Power Dissipation Average of Yield at Min and Max Lock Frequencies @ 1.0V (mW)	6.7-14.8	7.6-15.6
Phase Noise @ 1MHz (dBc/Hz)	-	-95
Fastest Lock Time (µs) 16GHz to 8GHz frequency step	2.3	2.6

Figure 17.6.6: Performance summary for HVT and RVT PLLs.

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